

Substrate gating of contact resistance in graphene transistors

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Metal contacts have been identified to be a key technological bottleneck for the realization of viable graphene electronics. Recently, it was observed that for structures that possess both a top and a bottom gate, the electron-hole conductance asymmetry can be modulated by the bottom gate. In this letter, we explain this observation by postulating the presence of an effective thin interfacial dielectric layer between the metal contact and the underlying graphene. Electrical results from quantum transport calculations accounting for this modified electrostatics corroborate well with the experimentally measured contact resistances. Our study indicates that the engineering of metal-graphene interface is a crucial step towards reducing the contact resistance for high performance graphene transistors.

Since its experimental isolation [1–3], graphene has attracted significant attention from the scientific community, due to its unique electronic structure and physical properties [4, 5]. Its excellent transport properties and the ability to tune the carrier concentration with electrical gates, also makes it a material with great technological promise. Potential applications range from RF devices and transistors [6–8] to bio-sensors [9] and flexible electronics [10]. The metal-graphene contact, is however, a key technological challenge for graphene-based electronic devices. For current-generation silicon metal-oxide-semiconductor field-effect transistors (MOSFETs), the International Technology Roadmap for Semiconductors calls for a resistance of $80\Omega\text{-}\mu\text{m}$ per contact, which is about 10% of the transistor's on-resistance V_{DD}/I_{ON} [11]. Graphene's excellent transport properties should produce transistor on-resistances considerably lower than those of silicon MOSFETs. To realize the performance potential afforded by the excellent transport properties of graphene, exceptionally low contact resistances will be required [6, 7]. It is, therefore, essential to develop a thorough understanding of metal-graphene contacts and of the fundamental lower limits for the contact resistance. In this paper, we develop a model that explains the recently observed substrate modulation of contact resistance in graphene transistors [12, 13]. We argue that this effect is due to the presence of an effective thin metal-graphene interfacial dielectric layer. Using this model, we estimate two important components of the series resistance and establish lower bounds for the contact resistance. The study provides an improved understanding of the metal-graphene contact that may prove useful for improving device performance.

Graphene is sensitive to external perturbations due to its all-surface and zero volume nature [9]. Charge transfer between metal and graphene due to a workfunction difference dopes the underlying graphene [14]. Contacts, therefore, introduce a built-in electrostatic junction within graphene, which was observed experimentally

using scanning tunneling microscopy [15]. A distinct experimental signature was the asymmetry of resistance in back-gated devices [16, 17]. The sign of this asymmetry reflects the doping of the graphene underneath the metal. Recently, devices with top and bottom gating schemes, as shown in Fig. 1, were experimentally realized [12, 13]. Measurement of resistance vs. top gate voltage (V_T) revealed an asymmetry, whose sign and magnitude were modulated by the back gate voltage (V_B). This observation strongly suggests that the graphene doping underneath the metal was substantially modulated by the back gate voltage.

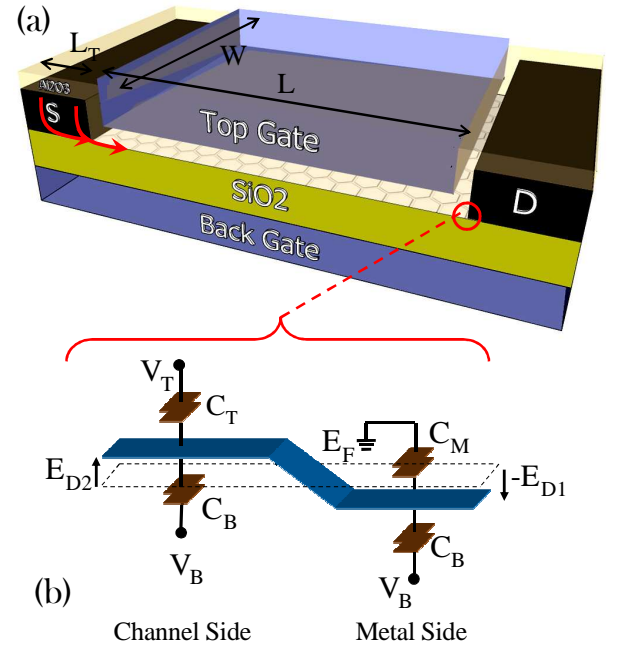


FIG. 1: (a) Top/bottom gated graphene structure, and (b) modeled potential profile across metal coated part and channel part of graphene sheet. With $C_T/(C_B)$ we denote the top/(bottom) gate capacitances, whereas C_M accounts for the interfacial capacitance between metal and graphene. The positive/(negative) sign of the difference $E_F - E_D$ between the Fermi level E_F and the Dirac surface E_D accounts for n/(p) doping of the respective region.

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It is instructive to recall that in standard metal-semiconductor junction theory, the Schottky barrier height is given by the difference between the metal workfunction, ϕ_M , and the electron affinity, χ_S , of the semiconductor, when there is no Fermi level pinning. However, the metal-graphene binding is comparatively weaker. The nature of the interfacial metal-graphene chemical bonding is still a subject of theoretical study [18]. Electrically, this interfacial layer can be modelled with an interfacial capacitance C_M . If $C_M \gg C_B$ and $C_M \gg C_{qm} \approx e^2 D(E_F - E_{D1})$, where D stands for the density-of-states, then one expects the Dirac point of graphene E_{D1} to be stationary with respect to ϕ_M . The above limit describes the standard metal-semiconductor junction, since C_M is generally significantly larger than the semiconductor capacitance. If $C_M \leq C_{qm}$, it is possible to modulate E_{D1} with an applied voltage V_B . Consideration of this fact is key to explaining the experimental results [12] of the device shown in Fig. 1.

The model: From Gauss's law, the electrostatic equations governing the graphene underneath the contact (region 1) and top gate (region 2) are

$$C_M(E_{D1} + \delta\phi) + C_B(E_{D1} - eV_B) = e^2 n_1 \quad (1)$$

$$C_T(E_{D2} - V_T) + C_B(E_{D2} - eV_B) = e^2 n_2, \quad (2)$$

where $\delta\phi \equiv \phi_M - \phi_G$ is the workfunction difference between metal and graphene, and $en_i = E_{Di}^2 / \pi(\hbar v_f)^2$. Note that E_F is taken to be zero as reference. The transition between region 1 and 2 is described by an analytical screening model [19], assuming a linear graded junction. The junction resistance, \mathcal{R}_{junc} , is then computed quantum mechanically using a previously developed mode space non-equilibrium Green function method for graphene [20]. For our ballistic study, the effect of temperature impacts our results only through the thermal smearing due to Fermi-Dirac distribution function, which is included in our study.

In the experiment [12], the gate capacitances are known, i.e. $C_B \approx 1.15 \times 10^{-4} \text{ F m}^{-2}$ and $C_T = 42C_B$. On the other hand, C_M is a quantity to be determined. Ti/Pd/Au is used for the metal contacts. For our calculations, we assumed $\delta\phi \approx 25 \text{ meV}$, a value that is sensible for our experimental metal stack [37]. Fig. 2a plots E_{D1} as a function of V_B and C_M . As expected, V_B modulates the doping in region 1, with greater ease when C_M is smaller. In the experiments, it was observed that the conductance as function of V_T exhibits the least asymmetry when $V_B \approx 10 \text{ V}$ (see Fig. 3a). This suggests that when $V_B \approx 10 \text{ V}$, $E_{D1} \approx 0$ (the charge neutrality point), which then also allows us to pin down C_M to be $C_M \approx 400C_B$. On the other hand, a different choice of $\delta\phi$ would correspondingly yield a different C_M , as illustrated in Fig. 2b.

Results: The measured conductance, $G(V_T)$, for different values of V_B is shown in Fig. 3a. The observed asymmetry in $G(V_T)$ changes sign at about $V_B = 10 \text{ V}$.

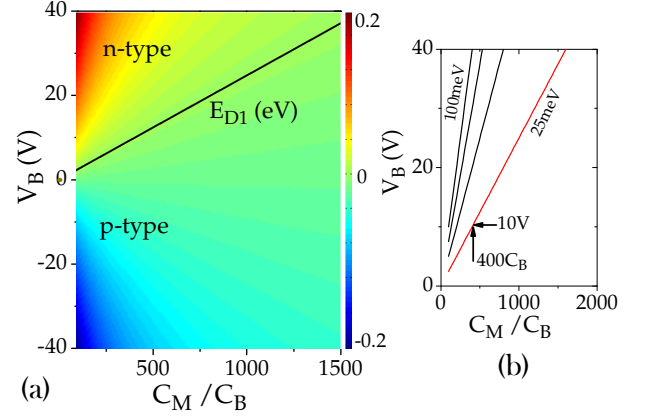


FIG. 2: (a) Surface potential (left), and (b) modulation of the neutrality condition (right) of the metal coated side of graphene. The doping of the metal coated side of graphene is modulated with the backgate V_B and depends also on the value of the interfacial capacitance C_M and the work function difference $\delta\phi$. The crossing line(s) in both figures reflect(s) zero surface potential (Dirac lines). In the inset (right), the modulation of the neutrality condition of the metal coated side of graphene is applied, in direct correspondence to the equation $C_M \delta\phi - C_B V_B = 0$

To facilitate comparison between experiment and a ballistic theory, we extract the odd component of the resistance [21] from experiment, given by $\mathcal{R}_{odd} \equiv \frac{1}{2}[\mathcal{R}(\delta V_T) - \mathcal{R}(-\delta V_T)]$, where δV_T is V_T with respect to the Dirac point voltage. The quantity \mathcal{R}_{odd} then allows for quantitative comparison between the experimentally measured $G(V_T)$ and the numerically calculated $\mathcal{R}_{junc}(V_T)$. Although interface charge, moisture, and chemicals in the vicinity may impact the transport properties of the graphene devices, these effects can be minimized by careful control of the fabrication process and the measurement conditions so that any asymmetry can be attributed entirely to the graphene p-n junction.

In Fig. 3b, the striking experimental observation of asymmetry inversion, as it is observed in \mathcal{R}_{odd} vs $V_B = -40 \text{ V}$ and $V_B = 40 \text{ V}$, is compared with our modeled \mathcal{R}_{odd} for a work function difference $\delta\phi = 0.025 \text{ eV}$ and an interfacial capacitance $C_M = 400C_B$. As elucidated previously, modulation of the doping of graphene underneath the metal is possible because C_M is not large enough to completely dominate over C_{qm} . In fact, for a moderate carrier concentration of $1 \times 10^{12} \text{ cm}^{-2}$, one obtains $C_{qm} \approx 0.75C_M$. If one assumes that the metal-graphene interfacial layer is an air gap, $C_M = 400C_B$ would then translate to a physical thickness of only 2 \AA . This is in good agreement with recent density functional studies [22], with a predicted metal-graphene binding distance of $\approx 3.5 \text{ \AA}$. The possibility of sign inversion is, however, conditional. For example, if we use a value of $C_M = 4000C_B$ instead of $C_M = 400C_B$, sign inversion of \mathcal{R}_{odd} would not be observed within the V_B range of interest, as shown in Fig. 3c. In Fig. 3d, we show that the increasing odd resistance with increasing $|V_B|$, as it

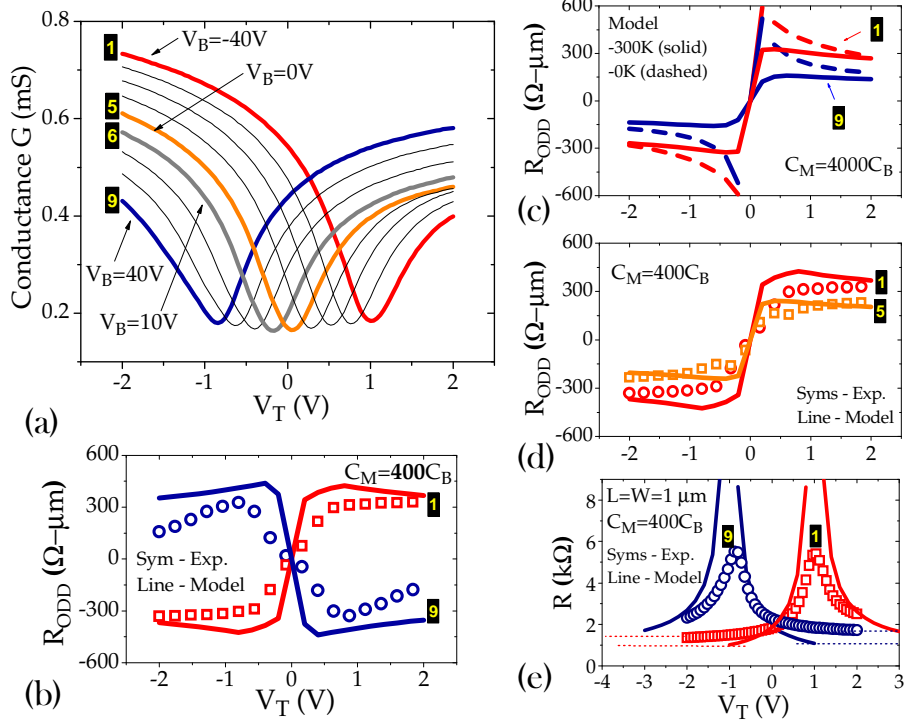


FIG. 3: Study of the conductance asymmetry of the Chen/Appenzeller experiments [12]. (a) Experimental $G - V_T$ curves for different back gate voltages V_B , ranging from $V_B = -40\text{ V}$ to $V_B = 40\text{ V}$. (b) Comparison of model prediction versus experiment for the odd part of resistance (\mathcal{R}_{odd}) vs top gate voltage V_T for $V_B = -40\text{ V}$ and $V_B = 40\text{ V}$, assuming an interfacial capacitance $C_M = 400C_B$, and a temperature of $T = 300\text{ K}$. (c) Model prediction of (\mathcal{R}_{odd}) for the same voltages for an elevated interfacial capacitance $C_M = 4000C_B$, for $T = 300\text{ K}$ (solid line) and $T = 0\text{ K}$ (dashed line). (d) Odd part of resistance (\mathcal{R}_{odd}) vs V_T for $V_B = 0\text{ V}$ and $V_B = -40\text{ V}$ with $C_M = 400C_B$ at $T = 300\text{ K}$. (e) Experimental $R - V_T$ curves for $V_B = -40\text{ V}$ and $V_B = 40\text{ V}$, versus our NEGF model, assuming an interfacial capacitance $C_M = 400C_B$, a work function difference $\delta\phi = 0.025\text{ eV}$ and a temperature of $T = 300\text{ K}$.

is observed in the experiment for $V_B = 0, -40\text{ V}$, can also be captured with our simulation, using $C_M = 400C_B$.

Up till now, we only considered \mathcal{R}_{junc} and its contribution to the asymmetric part of the contact resistance. Previous studies [23, 24] of the intrinsic transport properties of graphene on substrate allow one to make reasonable estimates of the channel resistance, \mathcal{R}_{cha} , by including contributions due to acoustic/optical phonons and substrate-induced remote phonons. However, their contributions relative to \mathcal{R}_{junc} are not as significant [38]. A modest mobility of $\approx 500\text{ cm}^2/\text{Vs}$ was extracted from the experiment in vicinity of the Dirac point, suggesting high levels of impurities [25]. Here, we model the impurity limited resistivity with the Laudauer formula using a mean-free-path proportional in energy i.e. $\rho_{im}^{-1} = h/2e^2 \times M^{-1}[L^{-1} + (\alpha E)^{-1}]$, where α is used to fit the mobility and M is the number of modes normalized to W . In Fig. 3e, we compare the experimental resistance with the calculated sum $\mathcal{R}_c = \mathcal{R}_{cha} + \mathcal{R}_{junc}$. By construction, our model does not capture the physics at the Dirac point. However, far away from the Dirac point, one observes an unaccounted for excess resistance in the experiment of $\approx 500\text{ }\Omega$, the origin of which is the subject

of subsequent discussion.

Other contributions to contact resistance include the current crowding effects due to access geometry and the presence of the metal-graphene interfacial layer. The latter implies that current has to tunnel across a dielectric layer, encapsulated in the electrical quantity $C_M = 400C_B$. The tunneling resistivity ρ_{tun} can be estimated using a model for quasi-bound electrons [26], commonly used in the study of gate leakage current in semiconductor inversion layers [27]. It is given by $\rho_{tun} = P\tau/e^2D$, where P is the Wentzel Kramers Brillouin tunneling probability estimated to be ≈ 0.3 , and τ is known as the classical bounce time [26], which in graphene is simply $\tau = 2t_g/v_f$, with t_g and v_f being the thickness of graphene and Fermi velocity respectively. Here, we take t_g to be the carbon-carbon bond length, $1.44\text{ }\text{\AA}$. This yields us a tunneling resistance estimate of $\rho_{tun} \approx 5.2 \times 10^{-6}\text{ }\Omega\text{-cm}^2$ for a pair of contacts. This value is reasonably close to a recently reported [28] experimental value of $\approx 5 \times 10^{-6}\text{ }\Omega\text{-cm}^2$.

Expanding the prior analysis to the spatial distribution of carrier flow, the current crowding effects due to the metal-graphene access geometry lead to an effective

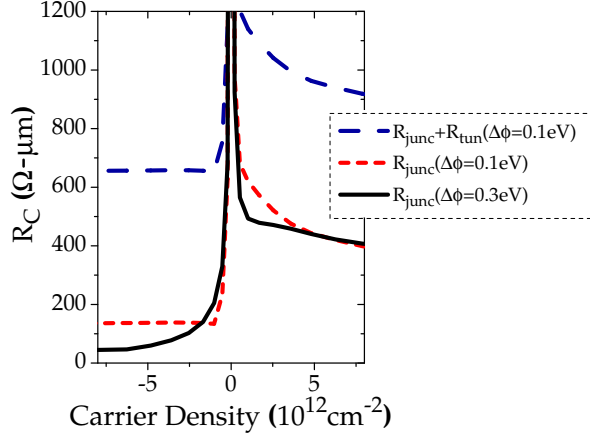


FIG. 4: Estimates of various components of contact resistance in graphene transistors. With the long-dashed line, we denote our modeled ballistic prediction for the junction resistance plus the tunneling resistance $\mathcal{R}_c = \mathcal{R}_{junc} + \mathcal{R}_{tun}$, for a pair of interfaces. After subtraction of \mathcal{R}_{tun} , we get the ballistic result for the lower bound of the contact resistance \mathcal{R}_{junc} (short-dashed line), assuming a work function difference $\phi_M - \phi_G = 0.1 \text{ eV}$. Last, an increase of the work function difference to $\phi_M - \phi_G = 0.3 \text{ eV}$ reduces further our ballistic prediction for the junction resistance \mathcal{R}_{junc} (solid line). (The region near $n_s = 0$ should be disregarded since it is strongly affected by spatial potential fluctuations, which are not considered in our model.)

electrical area for the contact where current flows, given simply by $W \times L_T$, where $L_T = \sqrt{\rho_c / \rho_g}$ is commonly known as the transfer length. With ρ_c and ρ_g , we denote the specific contact resistivity and the sheet resistance of the graphene layer underneath, respectively. Using our estimated $\rho_{tun} \approx 5.2 \times 10^{-6} \Omega\text{-cm}^2$ and a sheet resistance $\rho_g = 1660 \Omega/\square$ from the experiment [12], at a channel carrier concentration $n_s \approx 5 \times 10^{12} \text{ cm}^{-2}$, we find $L_T \approx 560 \text{ nm}$. Given the experiment to experiment variations in ρ_c and ρ_g , this value is within a reasonable range [28].

Perspective: Recently reported contact resistance values lie in the range $\mathcal{R}_c \approx 600 - 10^4 \Omega\text{-}\mu\text{m}$ [13, 28–32] (see Suppl. Info.). These values are considerably above what is required for high performance transistors [11]. In this section, we examine several issues related to the fundamental limit to \mathcal{R}_c .

In Fig. 4, we consider the contact resistance for a pair of interfaces \mathcal{R}_c , incorporating both the tunneling component $\mathcal{R}_{tun} = 520 \Omega$ that we extracted previously, and the junction component \mathcal{R}_{junc} assuming a work function difference $\phi_M - \phi_G = 0.1 \text{ eV}$ (long-dashed line). It is expected that \mathcal{R}_{tun} can vary considerably from experiment to experiment, due to different contact materials, interface conditions, etc. [13, 28–33]. Significant reduc-

tions in \mathcal{R}_{tun} will be crucial, and the contact metal and deposition and annealing conditions will be critical factors. Recently, it was demonstrated that a low power plasma O_2 treatment prior to metal deposition is beneficial in improving \mathcal{R}_{tun} [34]. Another very recent study demonstrates that \mathcal{R}_{tun} is temperature dependent, possibly due to an expansion of graphene-metal distance [33].

The ballistic junction component \mathcal{R}_{junc} , on the other hand, seems to have a more universal nature, since it is limited by the electrostatics condition, and the number of conducting channels bottleneck [20]. To illustrate this, we plotted \mathcal{R}_{junc} for $\phi_M - \phi_G = 0.1 \text{ eV}$ and 0.3 eV in Fig. 4. For channel carrier concentration $n_s < 0$, a lower resistance plateau forms. The resistance value of this plateau is described by the quantum contact resistance $R_Q = h/2e^2 \times M^{-1}W$ [35], where M is the number of current-carrying modes, and this limit is imposed by $\Delta\phi$ at the metal side of the junction. Indeed for $\Delta\phi = 0.1 \text{ eV}$ (short-dashed line), one finds $R_Q \approx 134 \Omega\text{-}\mu\text{m}$, while for $\Delta\phi = 0.3 \text{ eV}$ (solid line) one finds $R_Q \approx 45 \Omega\text{-}\mu\text{m}$. In the latter case, however, for moderate negative values of n_s , where the plateau hasn't been reached, quantum resistance R_Q is limited by the number of modes in the channel, and $R_Q = h/2e^2 \times 1/2\sqrt{\pi/n_s}$ holds valid instead. The elevated right branch, when $n_s > 0$, is due to the effect of interband tunneling. Selection of appropriate metal workfunction or approaches to engineer sharp p - n junction, i.e. chemical doping [6], are promising directions.

In conclusion, we have proposed a model that explains the gate dependent resistance asymmetry observed in experiments, and provides increased understanding of the different components of the contact resistance in graphene transistors. We show that the existence of an interfacial layer between the metal and graphene can explain the back gating of the contacts observed by Chen and Appenzeller [12]. The importance of such an interfacial layer to devices was also pointed out in two very recent studies. Robinson et al. show that residual photoresist following lithography can lead to high contact resistance [34], and Xia et al. explain the temperature dependence of the contact resistance in terms of the graphene to metal distance [33]. Our work and these studies point to the need for further understanding of the metal-graphene interfacial layer as a prerequisite for engineering a good contact resistance for graphene electronics.

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 - [37] Literature on metal workfunction on graphene reports wide range of $\delta\phi$, suggesting that experimental condition and surface physics introduce variability. Experiments have provided indication about the metal-graphene function difference, based on quantitative R_{ODD} analysis

[16], and photocurrent study [36]. From a computational standpoint, DFT studies [14, 14, 18] have provided support for a spectrum of work function differences in a range $\delta\phi = [-0.3, 0.5] \text{ eV}$ for several different metal compositions.

[38] For example, acoustic phonons limited resistivity is only 30Ω at room-temperature [23]. Since our device has an aspect ratio of $W/L = 1$. This contribution is not significant compared to \mathcal{R}_{junc} .